ADA-S9303
User Manual

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1 Introduction

The ADA-S9303 is a stand-alone RFSoC enclosure providing 16-RF analogue channels, Ethernet, RS232 Serial COM, USB, QSFP and GPIO. The RF channels can run up to 10GSPS (DAC) and 5 GSPS(ADC)

The ADA-S9303 uses a single 15V-24V input power supply. An on-board system monitor micro-controller provides voltage/current monitoring of the generated power supplies, as well as providing the capability to turn the supplies on/off via the micro USB interface. A USB to JTAG circuit is also provided, giving access to the JTAG chain without requiring an external JTAG box. Additionally, an on-board USB to UART converter circuit is also provided, removing the need for a dedicated USB to Serial cable.

1.1 Key Features

Key Features

- Xilinx RFSoC FPGA with PS block consisting of:
  - Quad-core ARM Cortex-A53, Dual-core ARM Cortex-R5, Mali-400 GPU
  - 1 bank of DDR4-2400 SDRAM 2GB
  - Two Quad SPI Flash memory, 512Mb each
  - USB
  - RS232 serial COM port
  - Gigabit Ethernet
- Programmable Logic (PL) block consisting of:
  - 4 HSSIO links to the QSFP connector
  - 2 banks of DDR4-2400 SDRAM, 1GB per bank
- RF Sampling block consisting of:
  - 8 12-bit 4/5GSPS RF-ADCs
  - 8 14-bit 6.5/10GSPS RF-DACs
  - 8 soft-decision FECs (ZU28DR/ZU48DR only)
  - 10MHz to 6GHz -3dB Bandwidth
  - Full Scale Input (100MHz): 5.5dBm
  - Full Scale Output (100MHz/20mA Mode): -2.0dBm
  - Full Scale Output (100MHz/32mA Mode/ZU48DR): 3.9dBm
- Front Panel IO Interface with:
  - 8 HF single ended ADC signals
  - 8 HF single ended DAC signals
  - Reference clock input for the RF sampling blocks
  - Reference clock output from RF sampling blocks
  - 2 digital GPIO

Figure 1 : ADA-S9303

ADMC-XMC-STANDALONE User Manual: https://www.alpha-data.com/xml//user_manuals/adc-xmc-standalone%20user%20manual_v2_0.pdf

ADM-XRC-9R1B User Manual: https://www.alpha-data.com/xml//user_manuals/adm-xrc-9r1-b%20user%20manual_v1_1.pdf

ADM-XRC-9R1B Reference Design: https://www.alpha-data.com/resource/admxrc9r1

2 Main Input Power Supply Requirements

The total power requirement will vary depending on the particular FPGA design. A 60W supply would likely be more than enough for most FPGA designs before thermal limits of the device and heatsink become the limiting factor. Alpha-Data can provide a power supply estimator spreadsheet to estimate the total power requirements for a particular FPGA design. An example compatible power supply is TT Electronics part number SW3479-VI: https://mou.sr/3DrPj5W

Spec	Value
Voltage	15V-24V
Power	60W
Current	5A Max.
Connector	2.1mm x 5.5mm DC power plug, centre pin positive

Table 1 : Suggested Input Supply Specifications

3 Installation and Power Up

1) Connect a USB cable to the micro-USB port. Alternatively, connect a serial cable to the serial port and connect the other end to a USB-to-serial converter.

2) Open a serial terminal at 115200 baud with 8 data bits, 1 stop bit.

3) Turn the power switch on, and the PS should start to boot from then internal SD card.

4) Once booted, login with the username "root" and password "root"

5) To run the RF example design, use the command "boardtest-9r1"

See the example design user guide for details on the operation of the boardtest-9r1 application

4 JTAG Interface

A USB to JTAG circuit is provided, giving access to the XMC JTAG interface without the need for an external programming box (e.g. Xilinx Platform Cable II). The USB to JTAG converter is compatible with Vivado, and will appear in hardware manager as a Digilent device.

5 USB to UART Interface

An on-board USB to UART circuit is provided, which allows the access to a serial terminal without the need to use a dedicated USB to Serial converter plus a serial cable. A multiplexer automatically selects between the USB and the D-SUB connectors to determine which transmits the serial data. The D-SUB port always has the priority and transmission data through the USB will be disabled if the COM port is active. Receiving data is always active for both ports.

6 Current/Voltage Monitoring

The ADA-S9303 provides current sense functionality on the 12V and combined 3V3 internal supplies. These values can be reported over the micro-USB interface, using the alpha-data "avr2util" utility.

Avr2util for Windows and the associated USB driver can be downloaded here:
https://support.alpha-data.com/pub/firmware/utilities/windows/

Avr2util for Linux can be downloaded here:
https://support.alpha-data.com/pub/firmware/utilities/linux/

Use "avr2util.exe /?" to see all options.
For example "avr2util.exe /usbcom \\.\com4 display-sensors" will display all sensor values.

Note that 'com4' is used here as an example, and should be changed to match the com port number assigned under windows device manager

7 On-Board Generated Power Supplies

The ADA-S9303 generates the 3V3/3V3_AUX/12V0/-12V0 supplies required by the XMC site from a single 15V-24V input supply. Each supply has the following specifications:

Power supply	Voltage (V)	Max. current (A)	Monitoring
3V3_DIG	3.3	9.3 [1]	Voltage and current [1]
3V3_AUX	3.3 [2]	0.2 [1]	Voltage and current [1]
12V0_DIG	12.0	5.0	Voltage and current

Table 2 : ADA-S9301 Power Supplies

[1] The 3V3_DIG and 3V3_AUX rails are generated from the same supply, so the maximum current is the combination of 3V3_AUX + 3V3_DIG. The current monitoring also measures the combined current.

[2] The 3V3_AUX rail is an always-on 3.3V auxiliary power supply from the 15V-24V input.

The 3V3_DIG/3V3_AUX/12V0_DIG current usage of a particular design can be estimated using a power estimation spreadsheet. Contact support@alpha-data.com for access to the spreadsheet.

8 Front-Panel I/O

The front panel interface consists of 20 SMA connectors. These connectors support an external reference clock input and output, two GPIO pins, 8 DAC signals and 8 ADC signals.

Figure 2 : Front Panel Pinout

Signal	Impedance (Ohms)	FPGA Pin Number	Signal Level
ADC0	50	AK2/AK1	-
ADC1	50	AH2/AH1	-
ADC2	50	AF2/AF1	-
ADC3	50	AD2/AD1	-
ADC4	50	AB2/AB1	-
ADC5	50	Y2/Y1	-
ADC6	50	V2/V1	-
ADC7	50	T2/T1	-
DAC0	50	N2/N1	-
DAC1	50	L2/L1	-
DAC2	50	J2/J1	-
DAC3	50	G2/G1	-
DAC4	50	E2/E1	-
DAC5	50	C2/C1	-
DAC6	50	B4/A4	-
DAC7	50	B6/A6	-
REF IN	50	-	3.3V
REF OUT	50	-	3.3V
EXTIO0	-	A14	3.3V
EXTIO1	-	B12	3.3V

Table 3 : Front panel I/O signals

9 Rear-Panel I/O

The rear panel interface consists of Power, USB, Ethernet, QSFP, RS-232 UART, GPIO and micro USB connectors.

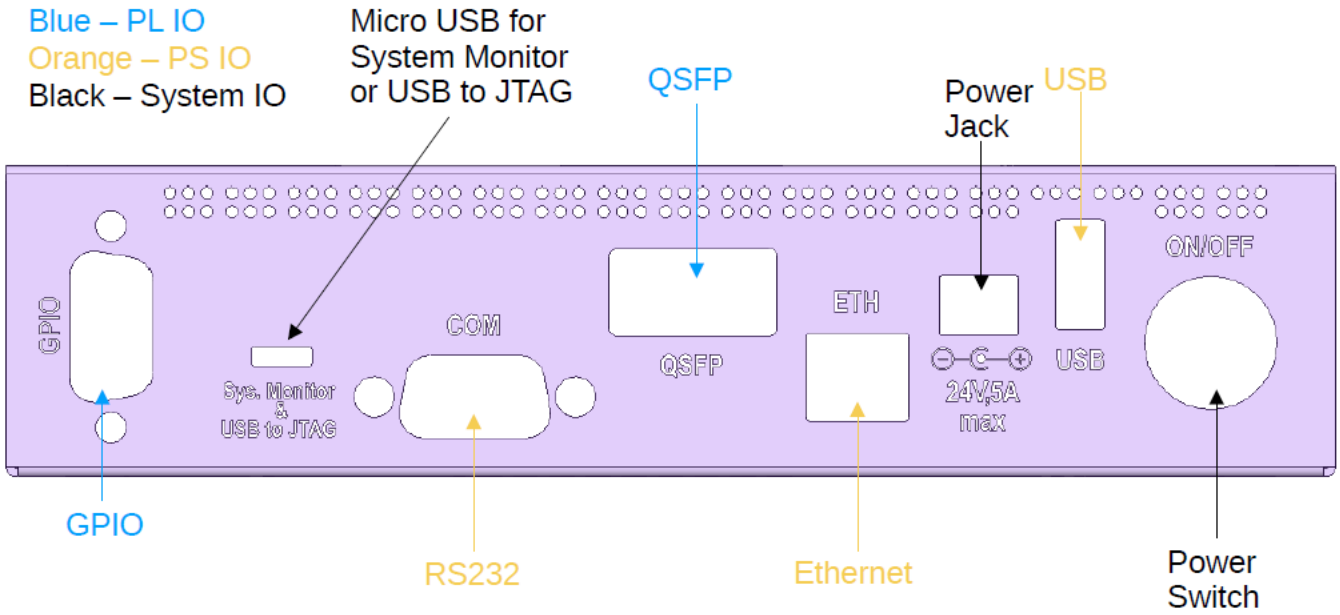

Figure 3 : Rear Panel Pinout

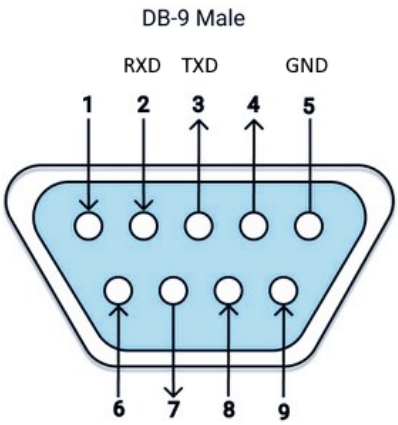

Figure 4 : RS-232 Pinout

10 QSFP pinout

The QSFP cage is connected to FPGA bank 129.

QSFP Lane	FPGA Bank 129 Lane
Tx0/Rx0	Tx3/Rx3
Tx1/Rx1	Tx2/Rx2
Tx2/Rx2	Tx1/Rx1
Tx3/Rx3	Tx0/Rx0

Table 4 : ADM-XRC-9R1-B pcb pinout for J16

11 GPIO pinout

The ADA-S9303 provides 8 GPIO (plus one ground pin) via its D-SUB connector.

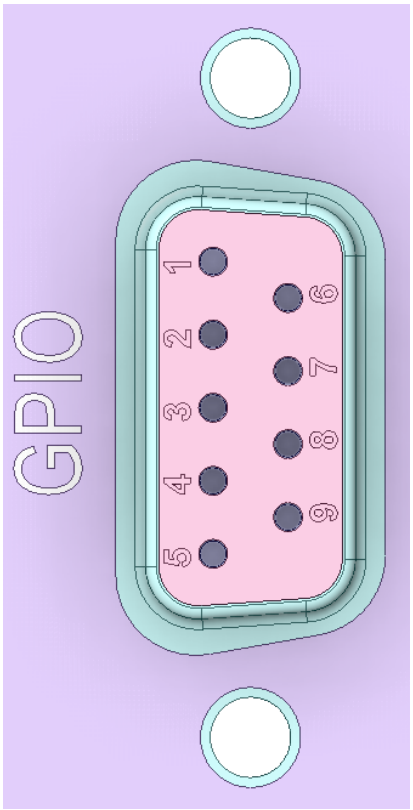

Figure 5 : GPIO DSUB Pin Numbers

DSUB Pin Number	FPGA Pin Number	Voltage Standard
1	D11	3.3V CMOS
2	E11	3.3V CMOS
3	A9	3.3V CMOS
4	B11	3.3V CMOS
5	N/A (GND)	N/A
6	E10	3.3V CMOS
7	K12	3.3V CMOS
8	C11	3.3V CMOS
9	C14	3.3V CMOS

Table 5 : GPIO pin mapping

12 Dimensions

Dimension	Measurement
Width	275mm
Depth	165mm
Height	48mm
Weight	1500g

Table 6 : ADS-STANDALONE/9R1 dimensions

13 Order Code

ADA-S9303/t/x/(f)

Option	Code	Description
XMC Connector type	t	blank = XMC (VITA 42) Connectors, /V88 = XMC+ (VITA 88) Connectors
FPGA Platform	x	9R1-B
RFSoC	f	27 = XCZU27DR-2, 28 = XCZU28DR-2, 47 = XCZU47DR-2, 48 = XCZU48DR-2

Table 7 : ADA-S9301 Order Code

Revision History

Date	Revision	Nature of Change
18 Dec 2024	1.0	First Release

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